PATENT

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**IN THE CLAIMS:**

*Please find a listing of the claims below, with the statuses of the claims shown in parentheses. This listing will replace all prior versions, and listings, of claims in the present application.*

1. (Currently amended) A data storage device comprising:

a storage medium comprising;

an electrode; [[and]]

an electrolyte layer positioned on the electrode; and

a conductive layer positioned on the electrolyte layer;

at least one probe configured to contact the conductive ~~electrolyte~~ layer, wherein the electrolyte conductive layer is positioned between the at least one probe and the electrolyte layer~~electrode~~; and

a voltage supply device configured to supply voltage through the at least one probe and the electrode to thereby create a circuit between the at least one probe and the electrode, wherein the level of voltage supplied by the at least one probe allows at least one of writing, reading, and erasing operations on one or more memory cells of the storage medium.

2. (Original) The device according to claim 1, wherein the electrode comprises one or more of gold, silver, copper, platinum, iridium, and palladium.

3. (Original) The device according to claim 1, wherein the electrolyte layer comprises a chalcogenide-metal composition.

4. (Original) The device according to claim 3, wherein the chalcogenide-metal composition comprises one or more of arsenic, germanium, selenium, sulfur, oxygen, tellurium, and antimony.

5. (Original) The device according to claim 3, wherein the chalcogenide-metal composition comprises one or more of silver, gold, platinum, palladium, copper, and iridium.

6. (Original) The device according to claim 1, wherein one or both of the storage medium and the at least one probe are movable with respect to each other.

7. (Currently amended) The device according to claim 1, ~~further comprising:~~ a wherein the voltage supplied comprises ~~supply device is configured to supply~~ a first voltage configured to perform a write operation in one or more memory cells of the storage medium, said first voltage being sufficiently high to form ~~a conductive path such as configuring a~~ metallic dendrites in the electrolyte layer at the locations of the one or more memory cells.

8. (Currently amended) The device according to claim 7, wherein the voltage supplied comprises ~~supply device is configured to supply~~ a second voltage configured to perform an erase operation in one or more memory cells of the storage medium, said second voltage having a reverse bias as compared to the first voltage, wherein the second voltage is operable to render a less conductive path in the electrolyte layer at the locations of the one or more memory cells.

9. (Currently amended) The device according to claim 8, wherein the voltage supplied comprises ~~supply device is configured to supply~~ a third voltage configured to perform a read operation on one or more memory cells of the storage medium, wherein the third voltage is a lower voltage than the first voltage or the second voltage and is sufficiently weak to cause little modification of the memory cell, said device further comprising:

a resistance measuring device configured to detect the resistance between the at least one probe and the electrode.

10. (Currently amended) The device according to claim 1, wherein the at least one probe comprises an inverted conical tip configured to contact the ~~electrolyte~~ conductive layer.

11. (Canceled).

12. (Currently amended) The device according to claim [[11]]1, wherein the conductive layer contains a metal comprising at least one of platinum, palladium, gold, iridium, silver, copper, and other materials that do not comprise or form insulating oxides.

13. (Currently amended) The device according to claim [[11]]1, wherein the conductive layer comprises a plurality of discrete conductive elements spaced apart from each other discontinuously, wherein the plurality of discrete conductive elements are associated with memory cells.

14. (Original) The device according to claim 13, wherein the electrode is sized and positioned to create an electric circuit with the plurality of discrete conductive elements.

15. (Currently amended) The device according to claim 14, ~~further comprising:~~ a wherein the voltage supplied comprises ~~supply device configured to supply~~ a first voltage configured to perform a write operation at the locations of the discrete conductive elements, said first voltage being sufficiently high to form ~~a conductive path such as configuring a~~ metallic dendrites in the electrolyte layer at the locations of the one or more memory cells associated with the discrete conductive elements.

16. (Currently amended) The device according to claim 15, wherein the voltage supplied comprises ~~supply device is configured to supply~~ a second voltage configured to perform an erase operation at the locations of the discrete conductive elements, said second voltage having a reverse bias as compared to the first voltage, wherein the second voltage is operable to render less conductive in the electrolyte layer at the locations of the one or more memory cells associated with the discrete conductive elements.

17. (Currently amended) The device according to claim 16, wherein the voltage supplied comprises ~~supply device is configured to supply~~ a third voltage configured to perform a read operation at the locations of the discrete conductive elements, wherein the third voltage is a lower voltage than the first voltage or the second voltage and is sufficiently weak to cause little modification of the memory cell, said device further comprising:

a resistance measuring device configured to detect the resistance between the at least one probe and the electrode at the locations of the one or more memory cells associated with the discrete conductive elements, said resistance being lower in those memory cells.

18. (Withdrawn) A method for storing data in a storage medium having an electrode and an electrolyte layer positioned on the electrode, said method comprising:

contacting at least one probe on the electrolyte layer, wherein the at least one probe is separate from the storage medium;

applying a voltage through the at least one probe at one or more memory cell locations such that one or more circuits are formed between the at least one probe and the electrode, wherein application of the voltage allows at least one of a writing, reading, and erasing operation on the one or more memory cells of the storage medium.

19. (Withdrawn) The method according to claim 18, wherein the step of applying a voltage comprises applying a first voltage having sufficient strength to form a conductive path such as configuring a metallic dendrite in the electrolyte layer to perform a writing operation at the locations of the one or more memory cells.

20. (Withdrawn) The method according to claim 19, wherein the step of applying a voltage comprises applying a second voltage having a reverse bias of the first voltage, said second voltage having sufficient strength to render less conductive in the electrolyte layer to perform an erasing operating at the locations of the one or more memory cells.

21. (Withdrawn) The method according to claim 20, wherein the step of applying a voltage comprises applying a third voltage having a lower strength than the first voltage or the second voltage, said third voltage also being sufficiently weak to cause little modification of the memory cell, said method further comprising:

determining the resistance between the at least one probe and the electrode to perform a reading operation at the locations of the one or more memory cells.

22. (Withdrawn) The method according to claim 21, wherein the step of determining the resistance further comprises assigning values to both of a higher resistance and a lower resistance, wherein the lower resistance is detected in the presence of a metallic dendrite at the locations of the one or more memory cells.

23. (Withdrawn) The method according to claim 22, wherein the step of assigning values comprises consistently assigning a "1" to the memory cells having metallic dendrites in the electrolyte layer and consistently assigning a "0" to other memory cells.

24. (Withdrawn) The method according to claim 22, wherein the step of assigning values comprises consistently assigning a "0" to the memory cells having metallic dendrites in the electrolyte layer and consistently assigning a "1" to other memory cells.

25. (Withdrawn) The method according to claim 18, said method further comprising:

moving one or both of the at least one probe and the storage medium with respect to each other to position the at least one probe over various ones of the one or more memory cells.

26. (Withdrawn) The method according to claim 18, wherein a conductive layer formed of discrete conductive elements is positioned on the electrolyte layer, and wherein the step of applying a voltage comprises applying a first voltage having sufficient strength to form a conductive path such as configuring a metallic dendrite in the electrolyte layer at the locations of the discrete conductive elements to perform a writing operation at the locations of the one or more memory cells associated with the discrete conductive elements.

27. (Withdrawn) The method according to claim 26, wherein the step of applying a voltage comprises applying a second voltage having a reverse bias of the first voltage, said second voltage having sufficient strength to render less conductive in the electrolyte layer to perform an erasing operating at the locations of the one or more memory cells associated with the discrete conductive elements.

28. (Withdrawn) The method according to claim 27, wherein the step of applying a voltage comprises applying a third voltage having a lower strength than the first voltage or the second voltage, said third voltage also being sufficiently weak to cause little modification of the memory cell, said method further comprising:

determining the resistance between the at least one probe and the electrode at the locations of the one or more memory cells associated with the discrete conductive elements to perform a reading operation at the locations of the one or more memory cells.

29. (Withdrawn) The method according to claim 28, wherein the step of determining the resistance further comprises assigning values to both of a higher resistance and a lower resistance, wherein the lower resistance is detected in the presence of a conductive path such as a metallic dendrite at the locations of the one or more memory cells associated with the discrete conductive elements.

30. (Withdrawn) The method according to claim 28, wherein the step of assigning values comprises consistently assigning a "1" to the memory cells associated with the discrete conductive elements having metallic dendrites in the electrolyte layer and consistently assigning a "0" to other memory cells.

31. (Withdrawn) The method according to claim 28, wherein the step of assigning values comprises consistently assigning a "0" to the memory cells associated with the discrete conductive elements having metallic dendrites in the electrolyte layer and consistently assigning a "1" to other memory cells.

32. (Withdrawn) The method according to claim 26, said method further comprising:

moving one or both of the at least one probe and the storage medium with respect to each other to position the at least one probe over various ones of the discrete conductive elements.

33. (Withdrawn) A system for storing data in one or more memory cells of a storage device with at least one probe, said one or more memory cells having an electrode and an electrolyte layer positioned on the electrode, said system comprising:

means for enabling contact between the at least one probe and the electrolyte layer; and

means for applying a voltage through the at least one probe such that a circuit is formed between the at least one probe and the electrode, wherein application of the voltage allows at least one of writing, reading, and erasing operations on the one or more memory cells of the storage medium.

34. (Withdrawn) The system according to claim 33, wherein the means for applying a voltage comprises means for applying a first voltage having a sufficient strength to form a conductive path such as configuring a metallic dendrite in the electrolyte layer to perform a writing operation in one or more memory cells.

35. (Withdrawn) The system according to claim 34, wherein the means for applying a voltage comprises means for applying a second voltage having a reverse bias of the first

voltage, said second voltage having sufficient strength to render less conductive in the electrolyte layer at the locations of the one or more memory cells to perform an erasing operation.

36. (Withdrawn) The system according to claim 35, wherein the means for applying a voltage comprises means for applying a third voltage having a lower strength than the first voltage or the second voltage, said third voltage also being sufficiently weak to cause little modification of the memory cell, said system further comprising:

means for determining the resistance between the at least one probe and the electrode to perform a reading operation on the one or more memory cells.

37. (Withdrawn) The system according to claim 36, wherein the means for determining the resistance comprises means for assigning values to both of a higher resistance and a lower resistance, wherein the lower resistance is detected in the presence of a conductive path such as a metallic dendrite at the locations of the one or more memory cells.

38. (Withdrawn) The system according to claim 37, wherein the means for assigning values is operable to consistently assign a "1" to the memory cells having conductive paths such as metallic dendrites in the electrolyte layer and to consistently assign a "0" to other memory cells.

39. (Withdrawn) The system according to claim 37, wherein the means for assigning values is operable to consistently assign a "0" to the memory cells having conductive paths such as metallic dendrites in the electrolyte layer and to consistently assign a "1" to other memory cells.

40. (Withdrawn) The system according to claim 33, said system further comprising:

means for moving one or both of the at least one probe and the storage medium with respect to each other to position the at least one probe over various ones of the one or more memory cells.

41. (Withdrawn) The system according to claim 33, wherein a conductive layer formed of discrete conductive elements is positioned on the electrolyte layer, and wherein the means for applying a voltage comprises means for applying a first voltage having a sufficient strength to form a conductive path such as configuring a metallic dendrite in the electrolyte layer at the locations of the discrete conductive elements to perform a writing operation in one or more memory cells associated with the discrete conductive elements.

42. (Withdrawn) The system according to claim 41, wherein the means for applying a voltage comprises means for applying a second voltage having a reverse bias of the first voltage, said second voltage having sufficient strength to render less conductive in the electrolyte layer at the locations of the one or more memory cells associated with the discrete conductive elements to perform an erasing operation.

43. (Withdrawn) The system according to claim 42, wherein the means for applying a voltage comprises means for applying a third voltage having a lower strength than the first voltage or the second voltage, said third voltage also being sufficiently weak to cause little modification of the memory cell, said system further comprising:

means for determining the resistance between the at least one probe and the electrode at the locations of the one or more memory cells associated with the discrete conductive elements to perform a reading operation on the one or more memory cells.

44. (Withdrawn) The system according to claim 43, wherein the means for determining the resistance comprises means for assigning values to both of a higher resistance and a lower resistance, wherein the lower resistance is detected in the presence of a conductive path such as a metallic dendrite at the locations of the one or more memory cells associated with the discrete conductive elements.

45. (Withdrawn) The system according to claim 44, wherein the means for assigning values is operable to consistently assign a "1" to the memory cells associated with the discrete conductive elements having conductive paths such as metallic dendrites in the electrolyte layer and to consistently assign a "0" to other memory cells.

46. (Withdrawn) The system according to claim 44, wherein the means for assigning values is operable to consistently assign a "0" to the memory cells associated with the discrete conductive elements having conductive paths such as metallic dendrites in the electrolyte layer and to consistently assign a "1" to other memory cells.

47. (Withdrawn) The system according to claim 33, said system further comprising:

means for moving one or both of the at least one probe and the storage medium with respect to each other to position the at least one probe over various ones of the discrete conductive elements.

48. (Withdrawn) A computer readable storage medium on which is embedded one or more computer programs, said one or more computer programs implementing a method for storing data in a storage medium having a an electrode and an electrolyte layer positioned on the electrode, said one or more computer programs comprising a set of instructions for:

contacting at least one probe on the electrolyte layer, wherein the at least one probe is separate from the storage medium;

applying a voltage through the at least one probe at the one or more memory cell locations such that one or more circuits are formed between the at least one probe and the electrode, wherein application of the voltage allows at least one of a writing, reading, and erasing operation on the one or more memory cells.

49. (Withdrawn) A computer readable storage medium on which is embedded one or more computer programs, said one or more computer programs implementing a method for storing data in a storage medium having a an electrode, a discontinuous conductive layer and an electrolyte layer positioned on the electrode, said one or more computer programs comprising a set of instructions for:

contacting at least one probe on the discontinuous conductive layer, wherein the at least one probe is separate from the storage medium;

applying a voltage through the at least one probe at the one or more memory cell locations such that one or more circuits are formed between the at least one probe and the electrode, wherein application of the voltage allows at least one of a writing, reading, and erasing operation on the one or more memory cells.

50. (New) An apparatus comprising:

a storage medium comprising,

an electrode;

an electrolyte layer positioned on the electrode; and

a conductive layer positioned on the electrolyte layer;

at least one probe configured to contact the conductive layer, wherein the conductive layer is positioned between the at least one probe and the electrolyte layer, and wherein the conductive layer is unconnected to a voltage source other than the at least one probe; and

a voltage supply device configured to supply voltage through the at least one probe and the electrode to thereby create a circuit between the at least one probe and the electrode, wherein the level of voltage supplied by the at least one probe allows at least one of writing, reading, and erasing operations on one or more memory cells of the storage medium.

51. (New) The apparatus according to claim 50, wherein the conductive layer comprises a plurality of discrete conductive elements spaced apart from each other discontinuously.

52. (New) The apparatus according to claim 50, wherein the at least one probe is movable with respect to the conductive layer.

53. (New) The device according to claim 50, wherein the voltage supplied comprises a first voltage configured to perform a write operation in one or more memory cells of the storage medium, said first voltage being sufficiently high to form metallic dendrites in the electrolyte layer at the locations of the one or more memory cells.

54. (New) The device according to claim 53, wherein the voltage supplied comprises a second voltage configured to perform an erase operation in one or more memory cells of the storage medium, said second voltage having a reverse bias as compared to the first voltage, wherein the second voltage is operable to render a less conductive path in the electrolyte layer at the locations of the one or more memory cells.

55. (New) The device according to claim 54, wherein the voltage supplied comprises a third voltage configured to perform a read operation on one or more memory cells of the storage medium, wherein the third voltage is a lower voltage than the first voltage or the second voltage and is sufficiently weak to cause little modification of the memory cell, said device further comprising:

a resistance measuring device configured to detect the resistance between the at least one probe and the electrode.

56. (New) A data storage device comprising:

a storage medium comprising;

an electrode;

an electrolyte layer positioned on the electrode; and

a plurality of discrete conductive elements positioned on the electrolyte layer, said plurality of discrete conductive elements being disconnected from each other and from a voltage source;

at least one probe configured to contact a selected one of the plurality of discrete conductive elements, wherein the selected one of the plurality of discrete conductive elements is positioned between the at least one probe and the electrolyte layer; and

a voltage supply device configured to supply voltage through the at least one probe, the selected one of the plurality of discrete conductive elements and the electrode to thereby create a circuit between the at least one probe and the electrode, wherein the level of voltage supplied by the at least one probe allows at least one of writing, reading, and erasing operations at a location of the selected one of the plurality of discrete conductive elements.

57. (New) The apparatus according to claim 56, wherein the at least one probe is movable with respect to the plurality of discrete conductive elements to thereby enable the at least one probe to address multiple ones of the plurality of discrete conductive elements.

58. (New) The device according to claim 56, wherein the voltage supplied comprises a first voltage configured to perform a write operation in one or more locations of the plurality of discrete conductive elements, said first voltage being sufficiently high to form

metallic dendrites in the electrolyte layer at the one or more locations of the plurality of discrete conductive elements.

59. (New) The device according to claim 58, wherein the voltage supplied comprises a second voltage configured to perform an erase operation in one or more locations of the plurality of discrete conductive elements, said second voltage having a reverse bias as compared to the first voltage, wherein the second voltage is operable to render a less conductive path in the electrolyte layer at the locations of the one or more plurality of discrete conductive elements.

60. (New) The device according to claim 59, wherein the voltage supplied comprises a third voltage configured to perform a read operation on one or more locations of the plurality of discrete conductive elements, wherein the third voltage is a lower voltage than the first voltage or the second voltage and is sufficiently weak to cause little modification of the electrolyte, said device further comprising:

a resistance measuring device configured to detect the resistance between the at least one probe and the electrode at one or more locations of the plurality of discrete conductive elements.